Crack resistant semiconductor package and method for making

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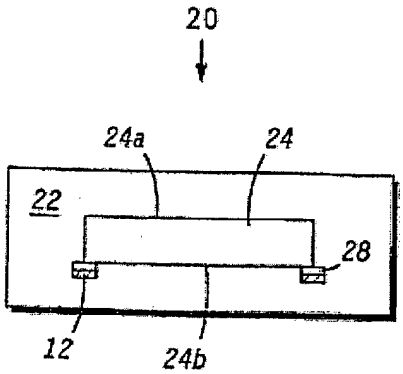
Abstract of **GB2261548**

A semiconductor package (20) includes a flagless leadframe having leads and a frame (12), and a semiconductor chip (24) having an upper surface (24a) and a lower surface (24b), wherein a portion of the lower surface (24b) is attached to the frame (12), and the upper surface (24a) and any exposed portion of the lower surface (24b) are substantially freed of carbon and carbon compounds. Residual carbon and carbon compounds are removed from the upper surface (24a) and the exposed portion of the lower surface (24b) by hydrogen flame or UV/ozone cleaning. A mold compound (22) encapsulates the semiconductor chip (24) and the leadframe except for leads which extend from the package (20).

FIG. 2



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Crack resistant semiconductor package and method for making

Description of **GB2261548**

CRACK RESISTANT SEMICONDUCTOR PACKAGE
AND METHOD FOR MAKING
Background of the Invention
This invention relates, in general, to semiconductor packages, and more particularly, to semiconductor packages which do not crack or delaminate when subjected to a thermal shock.

Semiconductor chips are often housed in surface mount plastic packages. Such packages comprise a semiconductor chip physically or mechanically attached to a leadframe and leads of the leadframe are selectively wire bonded to the semiconductor chip. The semiconductor chip and a portion of the leadframe are encapsulated by a mold compound. A problem with surface mount plastic packages is that they are prone to crack when the package is saturated with moisture and subjected to a thermal shock. These rather explosive failures have been calledpopcorn" failures due to the similarities of a popcorn kernel popping when subjected to heat.

Surface mount plastic packages are usually subjected to a thermal shock during soldering to a printed circuit board. The popcorn problem normally begins with the delamination of the flag-mold compound and the die bond-flag interfaces in the package. The delamination causes the package to swell and eventually crack. Preventing this delamination precludes popcorn failures. Delamination may be prevented by improving the adhesion between the flag-mold compound interface or the die bond-flag interface. Thus, the key to preventing popcorn problems is to prevent delamination by improving the adhesion at all interfaces in the package.

Attempts to solve the popcorn problem have not rendered a suitable solution to date. These attempts include improvements to the mold compound, improvements to the leadframe coatings and treatments, improvements in flag design features, and improvements in chip attach materials. Because these attempts have not prevented delamination, the current solution is to prevent the package from being exposed to moisture. This includes storing the semiconductor packages in dry packaging with a desiccant. The semiconductor packages must be kept dry until mounting to a printed circuit board. Solving the popcorn problem would result in a major cost savings by eliminating popcorn failures. In addition, it would not be necessary to store the semiconductor packages in a dry environment.

Summary of the Invention
Briefly stated, the present invention is achieved by a semiconductor package comprising a flagless leadframe having leads and a die opening, and a semiconductor chip having an upper surface and a lower surface, wherein a first portion of the lower surface is attached to the leadframe and a second portion of the lower surface is exposed by the die opening and is substantially free of carbon and carbon compounds.

Residual carbon and carbon compounds are removed from the exposed portion of the lower surface. A mold compound encapsulates the semiconductor chip and the leadframe except for leads which extend from the package.

Brief Description of the Drawings
FIG. 1 illustrates a top view of a portion of a leadframe used in the present invention; and
FIG. 2 illustrates an enlarged, cross-sectional view of an embodiment of the present invention.

-Detailed Description of the Preferred Embodiment
FIG. 1 illustrates a top view of an embodiment of a portion of a leadframe 10 of the present invention.

Leadframe 10 is comprised of tie bars 14 and a frame 12 having a central portion removed to provide die opening 11. A plurality of leads 13 surround frame 12 and are used to couple electric signals between a semiconductor device, described hereinafter, and external circuitry (not shown). This type of leadframe 10 has been termed "flagless." Advantages of using leadframe 10 are well known in the art and have been disclosed by Lesk et al in
U.S. Patent No. 4,924,291 issued on May 8, 1990, entitled "Flagless Semiconductor Package," which is incorporated herein by reference. Further details of how to fabricate leadframe 10 are found in the reference, as well as different embodiments which may be used.

FIG. 2 illustrates an enlarged, cross-sectional view of an embodiment in accordance with the present

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invention. A semiconductor package 20 comprised of an encapsulant 22 housing a semiconductor chip 24 which is physically or mechanically attached to frame 12 of leadframe 10. The mold compound only encapsulates a portion of leadframe 10 so that leads 13, shown in FIG.

1, extend from the package. In a preferred embodiment, a semiconductor chip 24 is attached to leadframe 10 by an epoxy or other polymer 28. Any suitable bonding method may be used.

It should be understood that the method of the present invention is useful for semiconductor packages using conventional leadframes which do not have a die op#ening 11, shown in FIG. 1. As described hereinafter, the present invention is useful in improving adhesion between surfaces of semiconductor chip 24 which contact encapsulant 22. Although improved adhesion is particularly useful in surface mount packages using flagless leadframe 10, improved adhesion also improves reliability and moisture resistance for any semiconductor device housed in a plastic package.

Semiconductor chip 24 has an upper surface 24a and a lower surface 24b. Lower surface 24b preferably comprises semiconductor material having no more than a native oxide. Semiconductor chip 24 may have either a polished or ground lower surface 24b. Optionally, lower surface 24b may comprise an inorganic dielectric layer such as silicon dioxide, silicon nitride, or the like.

In any case, it has been found that conventional assembly processes result in a residue on at least lower surface 24b. This residue comprises, among other things, carbon and carbon compounds deposited during wafer processing, sawing, and die bonding operations. In-particular, semiconductor chip 24 is usually mounted on an adhesive tape during saw operations before die-bond. This adhesive tape is believed to deposit significant quantities of carbon and carbon compound residue on lower surface 24b.

A first portion of lower surface 24b is physically or mechanically attached to frame 12 of leadframe 10 by epoxy 28, as set out hereinbefore. A second portion of lower surface 24b is exposed by die opening 11 and is in physical contact with encapsulant 22. It is believed that contaminants, especially carbon and carbon compounds, at the interface between encapsulant 22 and lower surface 24b result in poor adhesion at the interface which is a major cause of "popcorn" failures.

Thus, unlike conventional semiconductor package components, the package components in accordance with the present invention have a surface 24b which is substantially free of carbon and carbon compounds.

Furthermore, although delamination between upper surface 24a and encapsulant 22 is not strongly associated withpopcorn" failures, it is believed that making upper surface 24a free of carbon and carbon compounds will result in improved performance.

It is the combination of using flagless leadframe 10 and surface 24b which is substantially free of carbon residue that provides the advantages of the present invention. Even without using a flagless leadframe, however, it is believed that cleaning carbon residue from exposed surfaces such as upper surface 24a and edge surfaces will result in improved adhesion between the exposed surface and encapsulant 22. One method of removing carbon and carbon compounds from surface 24b is by exposing surface 24b to a hydrogen flame for a sufficient time to remove the carbon residue. Exposure to the hydrogen flame should occur shortly before encapsulation to ensure a clean surface 24b during encapsulation.

A preferred method for removing carbon residue is by exposing surface 24b to ultraviolet (UV) radiation in an oxygen and ozone atmosphere. This process, hereinafter referred to as UV/ozone cleaning, is a photosensitized oxidation process. Because oxidation of the carbon residue is enhanced by optical energy rather than thermal energy, UV/ozone cleaning is effective at much lower temperatures than hydrogen flame cleaning.

Lower temperatures simplify equipment design and processing. Low temperature processing also minimizes effect of the cleaning process on electrical characteristics of the semiconductor chip. UV/ozone cleaning is performed for a time sufficient to remove the carbon residue. In a typical process, cleaning time is about two to three minutes, although this time may vary significantly as a function of the quantity of residue which must be removed.

UV/ozone cleaning uses a conventional mercury (Hg) discharge lamp as a source of UV radiation. Hg discharge lamps have principle radiation output at 184.9 nanometers (nm) and 253.7 nm. The 184.9 nm output is absorbed by 2 molecules and creates atomic oxygen and ozone. Thus, the 184.9 nm output is principally responsible for creating the oxygen-ozone ambient which is used in the UV/ozone cleaning process. The 253.7 nm output serves to break molecular bonds of contaminant molecules, thus encouraging interaction of the contaminant molecules with the oxygen-ozone ambient. UV/ozone cleaning

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Crack resistant semiconductor package and method for making

Claims of **GB2261548**

CLAIMS

1. A method of making a crack resistant semiconductor package comprising the steps: providing a flagless leadframe having leads and a die opening; providing a semiconductor chip having an upper surface and a lower surface, wherein at least the lower surface has residual-carbon and carbon compounds thereon; attaching a first portion of the lower surface of the semiconductor chip to the flagless leadframe so that a second portion of the lower surface of the semiconductor chip is exposed; removing the residual carbon and carbon compounds at least from the lower surface; and encapsulating the semiconductor chip and the leadframe except for the leads which protrude therefrom.

2. The method of claim 1 wherein the step of removing the residual carbon and carbon compounds further comprises: providing a source of ultraviolet (UV) radiation; placing the flagless leadframe with the mounted semiconductor chip a predetermined distance from the source of UV radiation; and surrounding at least the lower surface with an oxygen and ozone atmosphere.

3. The method of claim 1 wherein the step of removing the residual carbon and carbon compounds further comprises: exposing the lower surface to ozone (03) and ultraviolet radiation.

4. The method of claim 1 further comprising removing carbon and carbon compounds from both the upper and lower surfaces before the step of encapsulating.

5. The method of claim 1 wherein the step of removing the residual carbon and carbon compounds further comprises: exposing the lower surface to a hydrogen flame.

6. The method of claim 1 further comprising the step of providing a dielectric layer on the lower surface of the semiconductor chip, wherein the residual carbon and carbon compounds are on the dielectric layer.

7. The method of claim 6 wherein the step of providing the dielecric layer comprises thermal oxidation of the lower surface to form silicon dioxide.

8. The method of claim 2 wherein the semiconductor chip further comprises a plurality of edge surfaces and the step of removing the residual carbon and carbon compounds further comprises exposing the plurality of edge surfaces to UV radiation and ozone.

9. A crack resistant semiconductor package component comprising: a semiconductor chip having an upper surface, a lower surface, and a plurality of edge surfaces; a flagless leadframe including leads and a die opening, the leadframe being mechanically bonded to a first portion of the lower surface and the die opening exposes a second portion of the lower surface, wherein the exposed second portion of the lower surface is substantially free of carbon and carbon compounds.

10. The crack resistant semiconductor package component of claim 9 further comprising an encapsulation disposed about the semiconductor die and the leadframe except for the leads which protrude therefrom, wherein the encapsulation is in physical contact with the exposed second portion of the lower surface.

11. The crack resistant semiconductor package component of claim 9 wherein the upper surface and the plurality of edge surfaces are substantially free of carbon and carbon compounds.

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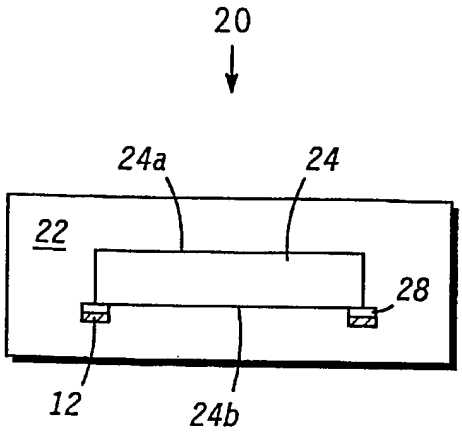
GB 1273589 A GB 1171467 A EP 0350021 A1

(58) Field of search
UK CL (Edition K) H1K KLX KPF KRA
INT CL[5] H01L

(54) **Crack resistant semiconductor package and method for making**

(57) A semiconductor package (20) includes a flagless leadframe having leads and a frame (12), and a semiconductor chip (24) having an upper surface (24a) and a lower surface (24b), wherein a portion of the lower surface (24b) is attached to the frame (12), and the upper surface (24a) and any exposed portion of the lower surface (24b) are substantially freed of carbon and carbon compounds. Residual carbon and carbon compounds are removed from the upper surface (24a) and the exposed portion of the lower surface (24b) by hydrogen flame or UV/ozone cleaning. A mold compound (22) encapsulates the semiconductor chip (24) and the leadframe except for leads which extend from the package (20).

FIG. 2



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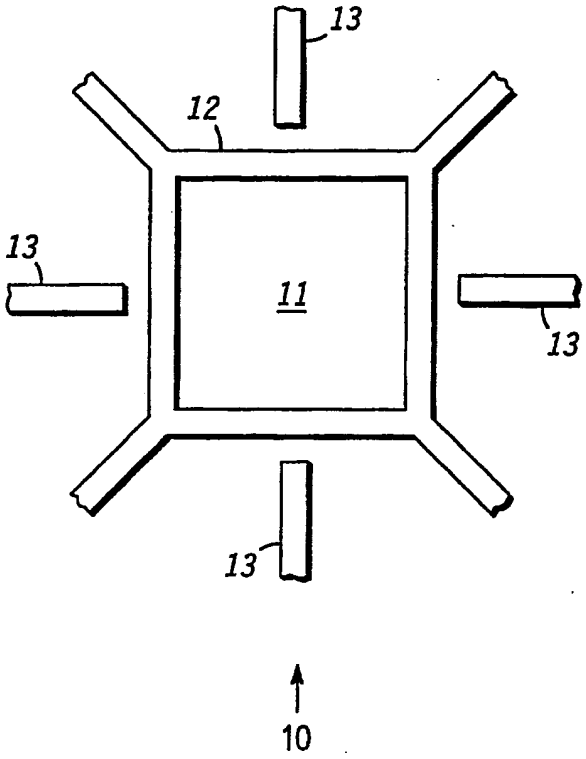
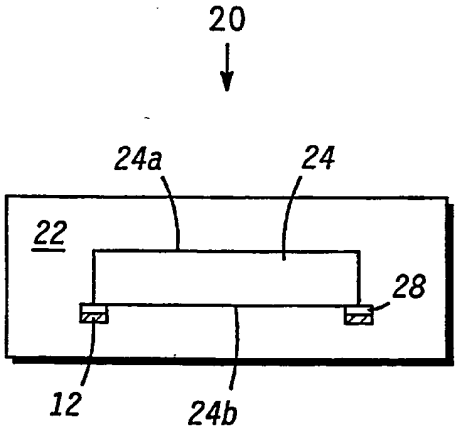


FIG. 1

FIG. 2



CRACK RESISTANT SEMICONDUCTOR PACKAGE AND METHOD FOR MAKING

Background of the Invention

This invention relates, in general, to semiconductor packages, and more particularly, to semiconductor packages which do not crack or delaminate when subjected to a thermal shock.

Semiconductor chips are often housed in surface mount plastic packages. Such packages comprise a semiconductor chip physically or mechanically attached to a leadframe and leads of the leadframe are selectively wire bonded to the semiconductor chip. The semiconductor chip and a portion of the leadframe are encapsulated by a mold compound. A problem with surface mount plastic packages is that they are prone to crack when the package is saturated with moisture and subjected to a thermal shock. These rather explosive failures have been called "popcorn" failures due to the similarities of a popcorn kernel popping when subjected to heat.

Surface mount plastic packages are usually subjected to a thermal shock during soldering to a printed circuit board. The popcorn problem normally begins with the delamination of the flag-mold compound and the die bond-flag interfaces in the package. The delamination causes the package to swell and eventually crack. Preventing this delamination precludes popcorn failures. Delamination may be prevented by improving the adhesion between the flag-mold compound interface or the die bond-flag interface. Thus, the key to preventing popcorn problems is to prevent delamination by improving the adhesion at all interfaces in the package.

Attempts to solve the popcorn problem have not rendered a suitable solution to date. These attempts include improvements to the mold compound, improvements to the leadframe coatings and treatments, improvements in flag design features, and improvements in chip attach materials. Because these attempts have not prevented delamination, the current solution is to prevent the package from being exposed to moisture. This includes storing the semiconductor packages in dry packaging with a desiccant. The semiconductor packages must be kept dry until mounting to a printed circuit board. Solving the popcorn problem would result in a major cost savings by eliminating popcorn failures. In addition, it would not be necessary to store the semiconductor packages in a dry environment.

Summary of the Invention

Briefly stated, the present invention is achieved by a semiconductor package comprising a flagless leadframe having leads and a die opening, and a semiconductor chip having an upper surface and a lower surface, wherein a first portion of the lower surface is attached to the leadframe and a second portion of the lower surface is exposed by the die opening and is substantially free of carbon and carbon compounds. Residual carbon and carbon compounds are removed from the exposed portion of the lower surface. A mold compound encapsulates the semiconductor chip and the leadframe except for leads which extend from the package.

Brief Description of the Drawings

FIG. 1 illustrates a top view of a portion of a leadframe used in the present invention; and

FIG. 2 illustrates an enlarged, cross-sectional view of an embodiment of the present invention.

Detailed Description of the Preferred Embodiment

FIG. 1 illustrates a top view of an embodiment of a portion of a leadframe 10 of the present invention. Leadframe 10 is comprised of tie bars 14 and a frame 12 having a central portion removed to provide die opening 11. A plurality of leads 13 surround frame 12 and are used to couple electric signals between a semiconductor device, described hereinafter, and external circuitry (not shown). This type of leadframe 10 has been termed "flagless." Advantages of using leadframe 10 are well known in the art and have been disclosed by Lesk et al in U.S. Patent No. 4,924,291 issued on May 8, 1990, entitled "Flagless Semiconductor Package," which is incorporated herein by reference. Further details of how to fabricate leadframe 10 are found in the reference, as well as different embodiments which may be used.

FIG. 2 illustrates an enlarged, cross-sectional view of an embodiment in accordance with the present invention. A semiconductor package 20 comprised of an encapsulant 22 housing a semiconductor chip 24 which is physically or mechanically attached to frame 12 of leadframe 10. The mold compound only encapsulates a portion of leadframe 10 so that leads 13, shown in FIG. 1, extend from the package. In a preferred embodiment, a semiconductor chip 24 is attached to leadframe 10 by an

epoxy or other polymer 28. Any suitable bonding method may be used.

It should be understood that the method of the present invention is useful for semiconductor packages using conventional leadframes which do not have a die opening 11, shown in FIG. 1. As described hereinafter, the present invention is useful in improving adhesion between surfaces of semiconductor chip 24 which contact encapsulant 22. Although improved adhesion is particularly useful in surface mount packages using flagless leadframe 10, improved adhesion also improves reliability and moisture resistance for any semiconductor device housed in a plastic package.

Semiconductor chip 24 has an upper surface 24a and a lower surface 24b. Lower surface 24b preferably comprises semiconductor material having no more than a native oxide. Semiconductor chip 24 may have either a polished or ground lower surface 24b. Optionally, lower surface 24b may comprise an inorganic dielectric layer such as silicon dioxide, silicon nitride, or the like. In any case, it has been found that conventional assembly processes result in a residue on at least lower surface 24b. This residue comprises, among other things, carbon and carbon compounds deposited during wafer processing, sawing, and die bonding operations. In particular, semiconductor chip 24 is usually mounted on an adhesive tape during saw operations before die-bond. This adhesive tape is believed to deposit significant quantities of carbon and carbon compound residue on lower surface 24b.

A first portion of lower surface 24b is physically or mechanically attached to frame 12 of leadframe 10 by epoxy 28, as set out hereinbefore. A second portion of lower surface 24b is exposed by die opening 11 and is in

physical contact with encapsulant 22. It is believed that contaminants, especially carbon and carbon compounds, at the interface between encapsulant 22 and lower surface 24b result in poor adhesion at the interface which is a major cause of "popcorn" failures. Thus, unlike conventional semiconductor package components, the package components in accordance with the present invention have a surface 24b which is substantially free of carbon and carbon compounds. Furthermore, although delamination between upper surface 24a and encapsulant 22 is not strongly associated with "popcorn" failures, it is believed that making upper surface 24a free of carbon and carbon compounds will result in improved performance.

It is the combination of using flagless leadframe 10 and surface 24b which is substantially free of carbon residue that provides the advantages of the present invention. Even without using a flagless leadframe, however, it is believed that cleaning carbon residue from exposed surfaces such as upper surface 24a and edge surfaces will result in improved adhesion between the exposed surface and encapsulant 22. One method of removing carbon and carbon compounds from surface 24b is by exposing surface 24b to a hydrogen flame for a sufficient time to remove the carbon residue. Exposure to the hydrogen flame should occur shortly before encapsulation to ensure a clean surface 24b during encapsulation.

A preferred method for removing carbon residue is by exposing surface 24b to ultraviolet (UV) radiation in an oxygen and ozone atmosphere. This process, hereinafter referred to as UV/ozone cleaning, is a photosensitized oxidation process. Because oxidation of the carbon residue is enhanced by optical energy rather

than thermal energy, UV/ozone cleaning is effective at much lower temperatures than hydrogen flame cleaning. Lower temperatures simplify equipment design and processing. Low temperature processing also minimizes effect of the cleaning process on electrical characteristics of the semiconductor chip. UV/ozone cleaning is performed for a time sufficient to remove the carbon residue. In a typical process, cleaning time is about two to three minutes, although this time may vary significantly as a function of the quantity of residue which must be removed.

UV/ozone cleaning uses a conventional mercury (Hg) discharge lamp as a source of UV radiation. Hg discharge lamps have principle radiation output at 184.9 nanometers (nm) and 253.7 nm. The 184.9 nm output is absorbed by O_2 molecules and creates atomic oxygen and ozone. Thus, the 184.9 nm output is principally responsible for creating the oxygen-ozone ambient which is used in the UV/ozone cleaning process. The 253.7 nm output serves to break molecular bonds of contaminant molecules, thus encouraging interaction of the contaminant molecules with the oxygen-ozone ambient. UV/ozone cleaning has also been found to remove contaminants such as phosphorous and nitrogen on the lower surface 24b, but these contaminants are normally in such low concentration on lower surface 24b that they are not believed to affect adhesion between encapsulant 22 and surface 24b.

It has been shown that a semiconductor package which is crack resistant can be fabricated by using a combination of a flagless leadframe and a cleaning process which removes carbon and carbon compounds from a lower surface of a semiconductor chip before encapsulation. This combination allows for exceptional adhesion to a mold compound, thus preventing cracking of

semiconductor packages during thermal shock. Improved adhesion also prevents contaminants from penetrating the semiconductor package, improving moisture resistance and durability of semiconductor devices even where a flagless leadframe is not used.

CLAIMS

1. A method of making a crack resistant semiconductor package comprising the steps: providing a flagless leadframe having leads and a die opening; providing a semiconductor chip having an upper surface and a lower surface, wherein at least the lower surface has residual carbon and carbon compounds thereon; attaching a first portion of the lower surface of the semiconductor chip to the flagless leadframe so that a second portion of the lower surface of the semiconductor chip is exposed; removing the residual carbon and carbon compounds at least from the lower surface; and encapsulating the semiconductor chip and the leadframe except for the leads which protrude therefrom.

2. The method of claim 1 wherein the step of removing the residual carbon and carbon compounds further comprises: providing a source of ultraviolet (UV) radiation; placing the flagless leadframe with the mounted semiconductor chip a predetermined distance from the source of UV radiation; and surrounding at least the lower surface with an oxygen and ozone atmosphere.

3. The method of claim 1 wherein the step of removing the residual carbon and carbon compounds further comprises: exposing the lower surface to ozone (O_3) and ultraviolet radiation..

4. The method of claim 1 further comprising removing carbon and carbon compounds from both the upper and lower surfaces before the step of encapsulating.

5. The method of claim 1 wherein the step of removing the residual carbon and carbon compounds further comprises: exposing the lower surface to a hydrogen flame.

6. The method of claim 1 further comprising the step of providing a dielectric layer on the lower surface of the semiconductor chip, wherein the residual carbon and carbon compounds are on the dielectric layer.

7. The method of claim 6 wherein the step of providing the dielecric layer comprises thermal oxidation of the lower surface to form silicon dioxide.

8. The method of claim 2 wherein the semiconductor chip further comprises a plurality of edge surfaces and the step of removing the residual carbon and carbon compounds further comprises exposing the plurality of edge surfaces to UV radiation and ozone.

9. A crack resistant semiconductor package component comprising: a semiconductor chip having an upper surface, a lower surface, and a plurality of edge surfaces; a flagless leadframe including leads and a die opening, the leadframe being mechanically bonded to a first portion of the lower surface and the die opening exposes a second portion of the lower surface, wherein the exposed second portion of the lower surface is substantially free of carbon and carbon compounds.

10. The crack resistant semiconductor package component of claim 9 further comprising an encapsulation disposed about the semiconductor die and the leadframe except for the leads which protrude therefrom, wherein

the encapsulation is in physical contact with the exposed second portion of the lower surface.

11. The crack resistant semiconductor package component of claim 9 wherein the upper surface and the plurality of edge surfaces are substantially free of carbon and carbon compounds.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

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Relevant Technical fields

(i) UK Cl (Edition K) H1K (KPF, KRA, KLX)

(ii) Int Cl (Edition 5) H01L

Search Examiner: W A MORRIS

Databases (see over)

(i) UK Patent Office

(ii)

Date of Search: 17.11.92

Documents considered relevant following a search in respect of claims ALL

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
A	EP 0350021 A2 (ENGLESBERG) see Example 1	1
X	GB 1273589 (TEXAS) see page 3 lines 3-9	1
X	GB 1171467 (NSC) see page 8 line 62 to page 9 line 52	1,4,9,11

Category	Identity of document and relevant passages	Relevant to claim(s.

Categories of documents

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